What is claimed is:

1. An ESD protection device comprising:
a substrate;
an isolation region on the substrate, enclosing an active region;
a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node;
a second gate disposed on a first side of the first gate and near the first end of the first gate; and
a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively, wherein the first doping region has a first gap under the second gate.

2. The ESD protection device as claimed in claim 1, wherein the isolation region is a shallow trench isolation.

3. The ESD protection device as claimed in claim 1, wherein the first node is ground while the second node is a pad.

4. The ESD protection device as claimed in claim 1 further comprising:
a third gate disposed on the first side of the first gate and near the second end of the first gate, wherein the first doping region has a second gap under the third gate.

5. The ESD protection device as claimed in claim 4 further comprising:

a fourth gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is between the first and fourth gate;

a fifth and sixth gate both disposed on a first side of the fourth gate, and respectively near a first and second end of the fourth gate, wherein the first doping region has a third and fourth gap respectively under the fifth and sixth gate; and

a third doping region on a second side of the fourth gate and coupled to the second node.

6. The ESD protection device as claimed in claim 5, wherein each of the second, third, fifth and sixth gate has one end overlapping the isolation region.

7 The ESD protection device as claimed in claim 5, wherein each of the first, second, third, fourth, fifth and sixth gate comprises:

a conducting layer;

a gate oxide layer under the conducting layer; and

a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

8. The ESD protection device as claimed in claim 7, wherein the conducting layer is a polysilicon layer while

the gate oxide layer, and the first and second spacer are silicon oxide layers.

9. The ESD protection device as claimed in claim 1 further comprising a fourth doping region enclosing the isolation region.

10. The ESD protection device as claimed in claim 9, wherein the substrate is a P substrate, the first, second and third doping region are N doping regions, and the fourth doping region is a P doping region.

11. An ESD protection device comprising:

a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node;

a second gate disposed on a second side of the first gate and near the first end of the first gate; and

a first and second doping region on a first and the second side of the first gate, and coupled to a second and the first node respectively, wherein the second doping region has a first gap under the second gate.

12. The ESD protection device as claimed in claim 11, wherein the isolation region is a shallow trench isolation.

13. The ESD protection device as claimed in claim 11, wherein the first node is ground while the second node is a pad.

14. The ESD protection device as claimed in claim 11 further comprising:

a third gate disposed on the second side of the first gate and near the second end of the first gate, wherein the second doping region has a second gap under the third gate.

15. The ESD protection device as claimed in claim 14 further comprising:

a fourth gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is between the first and fourth gate;

a fifth and sixth gate both disposed on a first side of the fourth gate, and respectively near a first and second end of the fourth gate; and

a third doping region on the first side of the fourth gate, coupled to the second node, and having a third and fourth gap respectively under the fifth and sixth gate.

16. The ESD protection device as claimed in claim 15, wherein each of the second, third, fifth and sixth gate has one end overlapping the isolation region.

17 The ESD protection device as claimed in claim 15, wherein each of the first, second, third, fourth, fifth and sixth gate comprises:

a conducting layer;

a gate oxide layer under the conducting layer; and

a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

18. The ESD protection device as claimed in claim 17, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

19. The ESD protection device as claimed in claim 11 further comprising a fourth doping region enclosing the isolation region.

20. The ESD protection device as claimed in claim 19, wherein the substrate is a P substrate, the first, second and third doping region are N doping regions, and the fourth doping region is a P doping region.

21. An ESD protection device comprising:

a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node; and

a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively, wherein the first doping region has a first gap near the first end of the first gate.

22. The ESD protection device as claimed in claim 21, wherein the isolation region is a shallow trench isolation.

23. The ESD protection device as claimed in claim 21, wherein the first node is ground while the second node is a pad.

24. The ESD protection device as claimed in claim 21, wherein the first doping region further has a second gap near the second end of the first gate.

25. The ESD protection device as claimed in claim 24 further comprising:

a second gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is on a first side of the second gate; and

a third doping region on a second side of the second gate, coupled to the second node;

wherein the first doping region has a third and fourth gap respectively near the first and second end of the second gate.

26. The ESD protection device as claimed in claim 25, wherein each of the first, second, third and fourth gap has one end connected to the isolation region.

27 The ESD protection device as claimed in claim 26, wherein each of the first and second gate comprises:

a conducting layer;

a gate oxide layer under the conducting layer; and

a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

28. The ESD protection device as claimed in claim 27, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

29. The ESD protection device as claimed in claim 21 further comprising a fourth doping region enclosing the isolation region.

30. The ESD protection device as claimed in claim 29, wherein the substrate is a P substrate, the first, second and third doping region are N doping regions, and the fourth doping region is a P doping region.

31. An ESD protection device comprising:

a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node; and

a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively, wherein the second doping region has a first gap near the first end of the first gate.

32. The ESD protection device as claimed in claim 31, wherein the isolation region is a shallow trench isolation.

33. The ESD protection device as claimed in claim 31, wherein the first node is ground while the second node is a pad.

34. The ESD protection device as claimed in claim 31, wherein the second doping region further has a second gap near the second end of the first gate.

35. The ESD protection device as claimed in claim 34 further comprising:

a second gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is on a first side of the second gate; and

a third doping region on a second side of the second gate, coupled to the second node;

wherein the second doping region has a third and fourth gap respectively near the first and second end of the second gate.

36. The ESD protection device as claimed in claim 35, wherein each of the first, second, third and fourth gaps has one end connected to the isolation region.

37 The ESD protection device as claimed in claim 36, wherein each of the first and second gates comprises:
a conducting layer;
a gate oxide layer under the conducting layer; and
a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

38. The ESD protection device as claimed in claim 37, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

39. The ESD protection device as claimed in claim 31 further comprising a fourth doping region enclosing the isolation region.

40. The ESD protection device as claimed in claim 39, wherein the substrate is a P substrate, the first, second and third doping region are N doping regions, and the fourth doping region is a P doping region.

41. An ESD protection device comprising:
a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node; and

a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively;

wherein the isolation region protruding into the first doping region near the first end of the first gate.

42. The ESD protection device as claimed in claim 41, wherein the isolation region is a shallow trench isolation.

43. The ESD protection device as claimed in claim 41, wherein the first node is ground while the second node is a pad.

44. The ESD protection device as claimed in claim 41, wherein the isolation region protruding into the first doping region near the second end of the first gate.

45. The ESD protection device as claimed in claim 44 further comprising:

a second gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is on a first side of the second gate; and

a third doping region on a second side of the second gate, coupled to the second node;

wherein the isolation region protruding into the first doping region near the first and second end of the second gate.

46. The ESD protection device as claimed in claim 45, wherein each of the first and second gate comprises:

a conducting layer;

a gate oxide layer under the conducting layer; and

a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

47. The ESD protection device as claimed in claim 46, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

48. The ESD protection device as claimed in claim 41 further comprising a fourth doping region enclosing the isolation region.

49. The ESD protection device as claimed in claim 48, wherein the substrate is a P substrate, the first, second and third doping regions are N doping regions, and the fourth doping region is a P doping region.

50. An ESD protection device comprising:

a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node; and

a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively;

wherein the isolation region protruding into the second doping region near the first end of the first gate.

51. The ESD protection device as claimed in claim 50, wherein the isolation region is a shallow trench isolation.

52. The ESD protection device as claimed in claim 50, wherein the first node is ground while the second node is a pad.

53. The ESD protection device as claimed in claim 50, wherein the isolation region protruding into the second doping region near the second end of the first gate.

54. The ESD protection device as claimed in claim 53 further comprising:

a second gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is on a first side of the second gate; and

a third doping region on a second side of the second gate, coupled to the second node;

wherein the isolation region protruding into the second doping region near the first and second end of the second gate.

55. The ESD protection device as claimed in claim 54, wherein each of the first and second gate comprises:
a conducting layer;
a gate oxide layer under the conducting layer; and
a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

56. The ESD protection device as claimed in claim 55, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

57. The ESD protection device as claimed in claim 50 further comprising a fourth doping region enclosing the isolation region.

58. The ESD protection device as claimed in claim 57, wherein the substrate is a P substrate, the first, second and third doping regions are N doping regions, and the fourth doping region is a P doping region.

59. An ESD protection device comprising:
a substrate;
an isolation region on the substrate, enclosing an active region;

a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node; and

a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively;

wherein the isolation region has a first portion under the first end of the first gate protruding into both the first and second doping region.

60. The ESD protection device as claimed in claim 59, wherein the isolation region is a shallow trench isolation.

61. The ESD protection device as claimed in claim 59, wherein the first node is ground while the second node is a pad.

62. The ESD protection device as claimed in claim 59, wherein the isolation region further has a second portion under the second end of the first gate protruding into both the first and second doping regions.

63. The ESD protection device as claimed in claim 62 further comprising:

a second gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is on a first side of the second gate; and

a third doping region on a second side of the second gate, coupled to the second node;

wherein the isolation region has a third and fourth portion respectively under the first and second protruding into both the first and second doping region.

64. The ESD protection device as claimed in claim 63, wherein each of the first and second gate comprises:
a conducting layer;
a gate oxide layer under the conducting layer; and
a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

65. The ESD protection device as claimed in claim 64, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

66. The ESD protection device as claimed in claim 59 further comprising a fourth doping region enclosing the isolation region.

67. The ESD protection device as claimed in claim 66, wherein the substrate is a P substrate, the first, second and third doping region are N doping regions, and the fourth doping region is a P doping region.

68. An ESD protection device comprising:
a substrate;
an isolation region on the substrate, enclosing an active region;

a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node;

a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively; and

a third doping region disposed under the first and second doping region and near the first end of the first gate, having a doping concentration lower than that of the first and second doping regions.

69. The ESD protection device as claimed in claim 68, wherein the isolation region is a shallow trench isolation.

70. The ESD protection device as claimed in claim 68, wherein the first node is ground while the second node is a pad.

71. The ESD protection device as claimed in claim 68 further comprising a fourth doping region disposed under the first and second doping regions and near the second end of the first gate, having a doping concentration lower than that of the first and second doping regions.

72. The ESD protection device as claimed in claim 71 further comprising:

a second gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein

the first doping region is on a first side of the second gate; and

a fifth doping region on a second side of the second gate, coupled to the second node;

wherein the third doping region is disposed under the first, second and fifth doping regions and near the first end of the first and second gate while the fourth doping region is disposed under the first, second and fifth doping regions and near the second end of the first and second gates.

73. The ESD protection device as claimed in claim 72, wherein each of the first and second gate comprises:

a conducting layer;

a gate oxide layer under the conducting layer; and

a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

74. The ESD protection device as claimed in claim 73, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

75. The ESD protection device as claimed in claim 68 further comprising a sixth doping region enclosing the isolation region.

76. The ESD protection device as claimed in claim 75, wherein the substrate is a P substrate, the first, second,

third, fourth and fifth doping region are N doping regions, and the sixth doping region is a P doping region.

77. An ESD protection device comprising:
a substrate;
an isolation region on the substrate, enclosing an active region;
a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node;
a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively; and
a first doping region well disposed under the first doping region and near the first end of the first gate.

78. The ESD protection device as claimed in claim 77, wherein the isolation region is a shallow trench isolation.

79. The ESD protection device as claimed in claim 77, wherein the first node is ground while the second node is a pad.

80. The ESD protection device as claimed in claim 77 further comprising a second doping region well disposed under the first doping region and near the second end of the first gate.

81. The ESD protection device as claimed in claim 80 further comprising:

a second gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is on a first side of the second gate; and

a third doping region on a second side of the second gate, coupled to the second node.

82. The ESD protection device as claimed in claim 81, wherein each of the first and second gates comprise:

a conducting layer;

a gate oxide layer under the conducting layer; and

a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

83. The ESD protection device as claimed in claim 82, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

84. The ESD protection device as claimed in claim 77 further comprising a fourth doping region enclosing the isolation region.

85. The ESD protection device as claimed in claim 84, wherein the substrate is a P substrate, the first, second and third doping regions are N doping regions, and the first and second doping regions are P doping regions.

86. An ESD protection device comprising:

a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node; and

a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively; and

wherein the first gate protruding into the first doping region so that, in the first doping region, a width of a center portion is larger than those of portions near the first and second end of the first gate.

87. The ESD protection device as claimed in claim 86, wherein the isolation region is a shallow trench isolation.

88. The ESD protection device as claimed in claim 86, wherein the first node is ground while the second node is a pad.

89. The ESD protection device as claimed in claim 86 further comprising:

a second gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is on a first side of the second gate; and

a third doping region on a second side of the second gate, coupled to the second node;

wherein the second gate protruding into the first doping region.

90. The ESD protection device as claimed in claim 89, wherein each of the first and second gate comprises:
a conducting layer;
a gate oxide layer under the conducting layer; and
a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

91. The ESD protection device as claimed in claim 90, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

92. The ESD protection device as claimed in claim 86 further comprising a fourth doping region enclosing the isolation region.

93. The ESD protection device as claimed in claim 92, wherein the substrate is a P substrate, the first, second and third doping region are N doping regions, and the fourth doping region is a P doping region.

94. A device without current crowding effect at the finger's ends, comprising:
a substrate;
an isolation region on the substrate, enclosing an active region;

a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node;

a second gate disposed on a first side of the first gate and near the first end of the first gate; and

a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively, wherein the first doping region has a first gap under the second gate.

95. The device as claimed in claim 94, wherein the isolation region is a shallow trench isolation.

96. The ESD protection device as claimed in claim 94, wherein the first node is ground while the second node is a pad.

97. The ESD protection device as claimed in claim 94 further comprising:

a third gate disposed on the first side of the first gate and near the second end of the first gate, wherein the first doping region has a second gap under the third gate.

98. The ESD protection device as claimed in claim 97 further comprising:

a fourth gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein

the first doping region is between the first and fourth gate;

a fifth and sixth gate both disposed on a first side of the fourth gate, and respectively near a first and second end of the fourth gate, wherein the first doping region has a third and fourth gap respectively under the fifth and sixth gate; and

a third doping region on a second side of the fourth gate and coupled to the second node.

99. The ESD protection device as claimed in claim 98, wherein each of the second, third, fifth and sixth gate has one end overlapping the isolation region.

100. The ESD protection device as claimed in claim 98, wherein each of the first, second, third, fourth, fifth and sixth gate comprises:

a conducting layer;

a gate oxide layer under the conducting layer; and

a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

101. The ESD protection device as claimed in claim 100, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

102. The ESD protection device as claimed in claim 94 further comprising a fourth doping region enclosing the isolation region.

103. The ESD protection device as claimed in claim 102, wherein the substrate is a P substrate, the first, second and third doping region are N doping regions, and the fourth doping region is a P doping region.